ABSTRACT OF THE DISCLOSURE

An image processing system whose circuit size is small, and whose dissipation power is small is provided. The image processing system executes digital image processing of an interval of active pixel in the condition that a first internal logic description is written in a field programmable gate array. Subsequently, in interval of non-active pixel with the exception of the interval of active pixel, the image processing system executes digital control processing in the condition that the first internal logic description of the field programmable gate array is rewritten to a second internal logic description. The image processing system executes again the digital image processing in the condition that the second internal logic description of the field programmable gate array is rewritten to the first internal logic description.